What is claimed is:

1. A lock detecting circuit that detects whether a PLL circuit is in a locked state based on a phase difference signal supplied from a phase comparator of the PLL circuit, the lock detecting circuit comprising:

a first circuit that outputs a control signal having one level when the phase difference signal does not indicate a generation of a phase difference, and the other level when the phase difference signal indicates a generation of a phase difference;

a second circuit that latches the control signal; and

a third circuit that outputs, for a predetermined second term, a lock detecting signal indicating that the PLL circuit is in a locked state, when the latched control signal indicates the one level for a predetermined first term.

2. The lock detecting circuit of claim 1, wherein

the third circuit measures a term during which the latched control signal continuously indicates the one level and, when the measured term exceeds the predetermined first term in length, outputs the lock detecting signal.

3. The lock detecting circuit of claim 1, wherein

the second term is set to be a term during which the latched control signal indicates the one level.

4. The lock detecting circuit of claim 2, wherein

the third circuit executes the measurement based on a second clock signal phase-inverted from a first clock signal that is used for the latching in the second circuit.

5. The lock detecting circuit of claim 4, wherein

the first and the second clock signals are clock signals created from an identical clock source.

6. The lock detecting circuit of claim 1, wherein

the third circuit outputs the lock detecting signal when the length of the term during which the latched control signal indicates the one level exceeds the length of a term during which the latched control signal indicates the other level, in a predetermined judgment term.

7. The lock detecting circuit of claim 1, wherein

the third circuit outputs the lock detecting signal when the length of the term during which the latched control signal indicates the one level exceeds the length of the first term that is set to be shorter in length than a predetermined judgment term, in the predetermined judgment

term.

8. A method for a lock detecting circuit to detect whether a PLL circuit is in a locked state based on a phase difference signal supplied from a phase comparator of the PLL circuit, the method comprising steps of:

creating a control signal that has one level when the phase difference signal does not indicate a generation of a phase difference, and that has the other level when the phase difference signal indicates a generation of a phase difference;

latching the control signal; and

outputting, for a predetermined second term, a lock detecting signal that indicates that the PLL circuit is in a locked state, when the latched control signal indicates the one level for a predetermined first term.